DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROGRAM AND SYLLABI

M.Tech
in
Microelectronics & VLSI

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NATIONAL INSTITUTE OF TECHNOLOGY

DURGAPUR-713209

CURRICULUM FOR THE M.TECH PROGRAMME

IN

MICROELECTRONICS & VLSI

2017

CONTENTS

1. Curriculum for M. Tech. in Microelectronics & VLSI

Department of Electronics and Communication Engineering

FIRST SEMESTER

Sl. No.	Course Code	Name of the Course/ Subject	L	T	S	C P
1.	EC1011	Semiconductor Device & Modeling	4	0	0	4
2.	EC1012	Analog IC Design	4	0	0	4
3.	EC1013	Digital IC Design	4	0	0	4
4.	***	Elective-I	4	0	0	4
5.	***	Elective-II	4	0	0	4
6.	EC1061	Design Lab-I	0	0	4	2
7.	EC1062	Design Lab-II	0	0	4	2
Total Credit:			**20**	**0**	**8**	**24**

SECOND SEMESTER

1.	EC2011	VLSI Technology	**4**	**0**	**0**	**4**
2.	EC2012	VLSI Systems Design	**4**	**0**	**0**	**4**
3.	***	Elective-III	**4**	**0**	**0**	**4**
4.	***	Elective-IV	**4**	**0**	**0**	**4**
5.	***	Elective-V	**4**	**0**	**0**	**4**
6.	EC2061	Design Lab-III	**0**	**0**	**4**	**2**
7.	EC2062	Project-I	**0**	**0**	**4**	**1**
8.	EC2063	Seminar (Non Project)				**1**
Total Credit:			**20**	**0**	**8**	**24**

THIRD SEMESTER

1.	EC3061	Project-II			**22**	**11**
2.	EC3062	Seminar			**04**	**02**
Total Credit:					**26**	**13**

FOURTH SEMESTER

1.	EC4061	Project-III			**22**	**11**
2.	EC4062	Seminar & Viva-Voce			**06**	**03**
Total Credit:					**28**	**14**
Total Credit:						**75**

2. Summary of the Curriculum

Semester	L	T	S	C	H
I	20	0	8	24	28
II	20	0	8	24	28
III	0	0	26	13	26
IV	0	0	28	14	28
Grand Total:	40	0	70	75	110
Grand Total (in %): [C / H]	**36.36**	**0**	**63.64**		

3. Distribution of the credit points and contact hours

A. Core Courses:

SI. No.	Course Code	Course Title	Credit	Hours
1.	EC1011	Semiconductor Device & Modeling	4	4
2.	EC1012	Analog IC Design	4	4
3.	EC1013	Digital IC Design	4	4
4.	EC2011	VLSI Technology	4	4
5.	EC2012	VLSI Systems Design	4	4
Total			**20**	**20**
Total (%)			**27.7%**	**18.2 %**

B. Elective Courses:

SI. No.	Course Code	Course Title	Credit	Hours
1.	EC90xx	Elective – I	4	4
2.	EC90xx	Elective – II	4	4
3.	EC90xx	Elective – III	4	4
4.	EC90xx	Elective – IV	4	4
5.	EC90xx	Elective – V	4	4
Total			**20**	**20**
Total (%)			**26.7 %**	**18.2 %**

C. Laboratory:

SI. No.	Course Code	Course Title	Credit	Hours
1.	EC1061	Design Lab I	2	4
2.	EC1062	Design Lab II	2	4
3.	EC2061	Design Lab III	2	4
Total			**6**	**12**
Total (%)			**8 %**	**10.9 %**

D. Project & Seminar:

SI. No.	Course Code	Course Name	Credit	Hours
1.	EC2062	Project-I	1	2
2.	EC2063	Seminar (Non-Project)	1	2
	EC3061	Project-II	11	22
3.	EC3062	Seminar	2	4
	EC4061	Project-III	11	22
4.	EC4062	Seminar & Viva-Voice	3	6
Total			**29**	**58**
Total (%)			**38.7 %**	**52.7 %**

4. List of Elective Courses:

Sl. No.	SUBJECT CODE	SUBJECT	L-T-P	CREDIT
1.	EC9011	COOPERATIVE COMMUNICATION NETWORK	4-0-0	4
2.	EC9012	STATISTICAL SIGNAL PROCESSING	4-0-0	4
3.	EC9013	OPTICAL COMMUNICATION	4-0-0	4
4.	EC9014	QUEUING THEORY FOR TELE- COMMUNICATION	4-0-0	4
5.	EC9015	SOFTWARE ENGINEERING	4-0-0	4
6.	EC9016	COMPUTER SIMULATION OF ELECTRONIC CIRCUITS	4-0-0	4
7.	EC9017	SPEECH SIGNAL PROCESSING	4-0-0	4
8.	EC9018	IMAGE PROCESSING	4-0-0	4
9.	EC9019	MICROPROCESSORS AND MICROCONTROLLER	4-0-0	4
10.	EC9020	NEURAL NETWORKS	4-0-0	4
11.	EC9021	DETECTION AND ESTIMATION THEORY	4-0-0	4
12.	EC9022	FIBRE OPTIC NETWORK	4-0-0	4
13.	EC9023	INFORMATION SECURITY AND CRYPTOGRAPHY	4-0-0	4
14.	EC9024	SATELLITE COMMUNICATION	4-0-0	4
15.	EC9025	MICROWAVE CIRCUITS AND TECHNIQUE	4-0-0	4
16.	EC9026	ADVANCED ANTENNA ARRAY SYNTHESIS	4-0-0	4
17.	EC9027	MICROWAVE MEASUREMENTS AND DESIGN	4-0-0	4
18.	EC9028	NETWORK INFORMATION THEORY	4-0-0	4
19.	EC9029	ANTENNA ANALYSIS AND SYNTHESIS	4-0-0	4
20.	EC9030	ARTIFICIAL INTELLIGENCE AND SOFT COMPUTING	4-0-0	4
21.	EC9031	VOICE AND PICTURE CODING	4-0-0	4
22.	EC9032	OPERATING SYSTEM	4-0-0	4
23.	EC9033	MATHEMATICAL METHOD IN TELECOMMUNICATION	4-0-0	4
24.	EC9034	DIGITAL SIGNAL PROCESSING & APPLICATION	4-0-0	4
25.	EC9035	TELECOMMUNICATION SYSTEM	4-0-0	4
26.	EC9036	EMBEDDED SYSTEMS	4-0-0	4
27.	EC9037	BROADBAND COMMUNICATION	4-0-0	4
28.	EC9038	ERROR CONTROL CODING	4-0-0	4
29.	EC9039	CAD FOR VLSI	4-0-0	4
30.	EC9040	VLSI FOR DIGITAL SIGNAL PROCESSING	4-0-0	4
31.	EC9041	MIXED SIGNAL IC DESIGN	4-0-0	4
32.	EC9042	LOW POWER CIRCUITS AND SYSTEMS	4-0-0	4
33.	EC9043	DSP ARCHITECTURES IN VLSI	4-0-0	4
34.	EC9044	RF IC DESIGN	4-0-0	4
35.	EC9045	SOC DESIGN	4-0-0	4
36.	EC9046	FPGA BASED DESIGN	4-0-0	4
37.	EC9047	MEMS & MICROSYSTEMS TECHNOLOGY	4-0-0	4
38.	EC9048	ARCHITECTURAL DESIGN IN IC	4-0-0	4
39.	EC9049	NANOELECTRONICS	4-0-0	4
40.	EC9050	COMPUTER ARCHITECTURE	4-0-0	4
41.	EC9051	TESTING AND VERIFICATION OF VLSI CIRCUITS	4-0-0	4

5. Assessment:

Laboratory Examination (40 + 40 + 20)

For the evaluation of Laboratory Courses, total 100 marks has three components

a) 40 marks for Continuous Assessment – which is based on the performance of the student on day to day basis in Laboratory and results obtained during the experiment done in the Laboratory. Attendance, general attentiveness/ behaviour of student and occasional instant quizzes are also considered in this component.
b) 40 marks for End-Semester Assessment– which has two subcomponents, 20 marks for performance of the students for experiment or program assigned to the students during the end-semester examination and 20marks for viva-voce examination.
c) 20 marks for Reports – which are written based on the laboratory experiments performed throughout the semester and during the end-semester examination.

Theory Examination

During 2017-2018 and 2018-2019, total 100 marks has three components

a) 20 marks for Continuous Assessment – which is based on quizzes, home assignments and surprise tests.
b) 30 marks for Mid-Semester Examination – which is conducted tentatively within 7-8 weeks after beginning of teaching in each semester.
c) 50 marks for End-Semester Examination – which is conducted at the end of teaching session of the semester.

Based on the feedback taken from the concerned stakeholders of the Institute, PG curriculum has been revised in the academic year 2019-2020. In the new curriculum the evaluation process for the theory subjects is changed as follows.

Continuous assessment 1 (15 marks)

This is realized with class tests, quizzes, home assignments, surprise tests or a combination of these components. If more than two class tests are conducted, the marks are averaged.

Continuous assessment 2 (25 marks, 2 hours)

Mid-term examination covers half of the syllabus. The exam is conducted at the middle of the semester following the academic calendar. The evaluation is done within a fortnight and the answer scripts are shown to the students so that they can understand their shortcomings in learning the subject.

End-term examination (60 marks, 3 hours)

End-term examination covers the full syllabus. The exam is centrally conducted at the end of the semester. After the evaluation, the answer scripts are shown to the students. Model answers are also provided.

6. Program Outcomes (POs) and Program Specific Outcomes (PSOs)

I. Program Outcomes (Pos):

NBA has defined the following three POs for the PG programs:

PO 1: An ability to independently carry out research /investigation and development work to solve practical problems

PO 2: An ability to write and present a substantial technical report/document

PO 3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program

II. Program Specific Outcomes (PSOs):

In addition to the three POs, 3 program specific outcomes (PSOs) have been defined by the Department as follows -

PSO 1 (PO 4): Identify, formulate and solve engineering problems in the field of Microelectronics and VLSI

PSO 2 (PO 5): Apply knowledge, proper methodology and modern tools to analyse and solve the problems in the domain of Microelectronics and VLSI.

PSO 3 (PO 6): Acquire professional and intellectual integrity and ethics of research and recognize the need to engage in learning with a high level of enthusiasm and commitment to contribute to the community for sustainable development of society

Course Articulation Matrices: Connection between the courses and the POs and PSOs

The correlation levels are 1, 2 or 3, denoting:
1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High).

Note: Other than the above-mentioned courses, any course including core and elective offered by another PG program of the Department / Institute can be opted as elective subjects without any constraint.

7. DETAILED SYLLABIOF THE COURSES

A. Core Courses

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours : 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC1011</td><td>Semiconductor Device & Modeling</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites:</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">B.Tech/B.E. with good background in Semiconductor Devices</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To introduce the principles of devices with emphasis to MOS and nano-device operations this is extremely important to the design of any VLSI circuit.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: To introduce the physics of semiconductor materials for understanding the device modeling of semiconductor devices.
CO#2: To understand the transport of charge carriers for the operation of semiconductor devices.
CO#3: To apply suitable approximations and techniques to derive the physical model of semiconductor devices such as P-N junctions.
CO#4: To analyze electrostatic variables and current-voltage characteristics of MOS devices under a variety of conditions.
CO#5: To evaluate qualitative understanding of the physics of emerging MOS devices and conversion of this understanding into modeling.
CO#6: To develop the fundamental understanding of device modeling and numerical simulation</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 08)
SEMICONDUCTOR ELECTRONICS: Physics of Semiconductor Materials, Band Model of Solids, Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Hall-Effect.

Module-II: (L – 06)
METAL-SEMICONDUCTOR CONTACTS and PN JUNCTIONS: Metal-Semiconductor junctions, Current-Voltage Characteristics, Surface Effects. The PN junction, Step Junction, Linearly Graded junction, Heterojunctions, Reverse-Biased PN junctions and breakdown mechanism. Generation and Recombination.</td></tr>
</table>

	Module-III: (L – 08) FIELD-EFFECT TRANSISTORS (MOSFETs): PHYSICAL EFFECTS AND MODELS:MOS Capacitor, Flat Band Voltage, Oxide and Interface Charge, High and Low Frequency C-V Characteristics: Origin and Experimental Determination. Charge- Coupled Devices, non-volatile memory. Basic MOSFET behavior, MOSFET scaling and short channel behavior. Devices: Complementary MOSFETs (CMOS), electric fields and velocity-saturation, basic leakage currents, channel length modulation, body bias effect, threshold adjustment, sub-threshold conduction. **Module-IV: (L – 08)** Short Channel Effects: Limitation of long channel analysis, short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, hot carrier effects, MOSFET scaling goals, gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current and other effects in scaled MOSFETS. Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, nonconventional MOSFET- (FDSOI, SOI, Multi-gate MOSFET) **Module-V: (L – 05)** Modeling: SPICE transistor modeling, compact MOSFET modeling approaches, history of BSIM models, BSIM family of Compact device models, BSIM6 model, BSIM-CMG model, BSIM-IMG model, physics of nanoscale MOSFET, and Design issues of nanoscale MOSFET: challenges of nanoscale MOSFET, scaling trends of MOSFETs, issues for nanoscale MOSFETs (short channel effects), key issues in modeling of MOSFET. **Module-VI: (L – 05)** Numerical Simulation: Numerical simulation, basic concepts of simulations, grids, device simulation and challenges. Importance of semiconductor device simulators - Key elements of physical device simulation, historical development of the physical device modeling. Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations – MOSFETs and SOI
Text / Ref. Books	Text Books: 1. Advanced Semiconductor Devices by Taur and Ning. 2. Device Electronics for Integrated circuits by Muller and Kammins. 3. Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation by Dr. Vagica Vasileska and Stephen M. Goodnick. 4. Semiconductor Device Modelling by A B. Bhattacharyya. References: 1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, 3rd Edition, (John Wiley & Sons, 2002). 2. Semiconductor Device Fundamentals by Robert F. Pierret, Addison-Wesley Publishing, 1996 3. Semiconductor Physics and Devices by Donald A. Neamen, 3rd Edition, Mc Graw Hill, 2003 4. Semiconductor Devices- Basic Principles", by Jasprit Singh, John Wiley and Sons Inc., 2001

EC 1011: Semiconductor Device Modeling (Core)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	To introduce the physics of semiconductor materials for understanding the device modeling of semiconductor devices.	1	1	3	2	1	1
CO 2	To understand the transport of charge carriers for the operation of semiconductor devices.	2	1	3	2	1	1
CO 3	To apply suitable approximations and techniques to derive the physical model of semiconductor devices such as P-N junctions.	2	2	3	2	3	1
CO 4	To analyse electrostatic variables and current-voltage characteristics of MOS devices under a variety of conditions.	2	2	3	3	2	1
CO 5	To evaluate qualitative understanding of the physics of emerging MOS devices and conversion of this understanding into modeling.	2	2	3	3	3	2
CO 6	To develop the fundamental understanding of device modeling and numerical simulation	3	3	3	3	3	2
Average		**2**	**1.83**	**3**	**2.5**	**2.17**	**1.33**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC1012</td><td>Analog IC Design</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites / Co-requisites</td><td colspan="5">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="3">Semiconductor Devices, Analog Circuit Design</td><td colspan="5">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objective</td><td colspan="7">To lay good foundation on the design and analysis of CMOS analog integrated circuits and expose the students to the fundamentals of Analog IC design.</td></tr>
<tr><td>Course Outcomes

After going through the course, student will be able to</td><td colspan="7">CO#1: Analyze MOSFET based circuits
CO#2: Draw the small signal models of MOS transistors
CO#3: Design basic Amplifiers using CMOS
CO#4: Illustrate the operation of a Differential amplifier
CO#5: Compute the frequency response of the amplifiers
CO#6: Identify the various design metrics of analog Design.
CO#7: Compare different types of Layout followed in Analog IC Design</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 05)
MOSFET Operation & Model: Device Structure I/V characteristics, second order effects, Capacitances, body bias effect, DIBL, MOS small signal Models, CMOS Technology

Module-II: (L – 06)
Basic Analog blocks: Basic concepts of amplification and biasing, Current sources and sinks, Current mirrors: Simple current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Current conveyer.

Module-III: (L – 07)
Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stage with source degeneration, source follower, CG stage, Gain boosting techniques, cascode, folded cascode.

Module-IV: (L – 07)
Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion. Differential amplifier-characterization, ICMR, Slew Rate, PSRR, offset,

Module-V: (L – 07)
Frequency response of Amplifiers: Device high-frequency small-signal models; Device capacitances, ft calculation, Simplified high-frequency analysis of basic amplifiers, Miller's theorem, OCTC method for BW estimation. cascode amplifiers, differential amplifiers.

Module-VI: (L – 04)
Feedback Amplifier: Feedback concept, negative & positive feedback, voltage/ current, series/shunt feedback, Practical feedback circuits, Loop gain and stability, Design</td></tr>
</table>

	Procedure for the feedback amplifiers. **Module-VII: (L – 04)** **Layout:** Introduction to Layout, Fingering, Inter-digitization, Common Centroid, Process gradients, electro-migration and antenna effect
Text Books, and/or Reference material	Text Books: 1. Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill 2. Analysis and Design of Analog Integrated Circuit, Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, John Wiley & Sons 3. Adel S. Sedra, Kenneth C. Smith : Microelectronics Circuits, Oxford University Press
	Reference Books/materials: 1. R. L.. Geiger, Allen and Stradder, VLSI Design Techniques for Analog and Digital Circuits, McGraw-Hill Education, 2010. 2. CMOS: Circuit Design, Layout, and Simulation by R. Jacob Baker, Wiley-IEEE Press(2019)

EC 1012: Analog IC Design (Core)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Analyze MOSFET based circuits.	2	1	2	1	1	1
CO 2	Draw the small signal models of MOS transistors.	2	2	3	2	2	1
CO 3	Design basic Amplifiers using CMOS.	2	2	3	3	2	1
CO 4	Illustrate the operation of a Differential amplifier.	2	2	3	3	3	1
C0 5	Compute the frequency response of the amplifiers.	2	2	3	3	3	1
CO 6	Identify the various design metrics of analog Design.	2	2	3	3	2	1
Co 7	Compare different types of Layout followed in Analog IC Design.	2	2	3	3	2	1
Average		**2**	**1.86**	**2.86**	**2.57**	**2.14**	**1**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC1013</td><td>Digital IC Design</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="2">Digital Circuits and Systems</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To study the characteristics of CMOS inverter, interconnects, combinational and sequential circuits and knowledge on Electronic Design Automation (EDA) tools in VLSI and experiment with the current technology/process, and able to design state-of-the-art CMOS circuits.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Acquire idea about the digital IC design techniques.
CO#2: Understand the characteristics of CMOS inverter.
CO#3: Learn the basic steps of ASIC Design Flow and fabrication process.
CO#4: Analyze the static and dynamic characteristics of CMOS circuits
CO#5: Design and implementation of combinational and sequential circuits
CO#6: Evaluate the performance of CMOS circuits</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I:(L –02)
Overview of VLSI Design: Historical perspective, overview of VLSI design methodologies, VLSI design flow, design hierarchy, concepts of regularity, modularity, and locality, VLSI design styles, design quality, packaging technology, CAD technology.

Module-II:(L –03)
MOS Transistor Theory: Introduction to The metal oxide semiconductor (MOS) structure, Long-channel I-V characteristics, C-V characteristics, non-linear I-V effects, DC transfer characteristics.

Module-III(L – 06)
ASIC Design Flow:
Introduction to ASIC and SoC, Overview of ASIC flow, functional verification, RTL-GATE level synthesis, synthesis optimization techniques, pre-layout timing verification, static timing analysis, floor-planning, placement and routing, extraction, post layout timing verification, extraction.

Module-IV:(L –02)
CMOS Process Technology: Fabrication process flow- basic steps, the CMOS n-Well process, layout design rules, stick diagram, full-custom mask layout design.

Module-V:(L –04)
MOS Inverter (Static Characteristics): Resistive-load inverter, inverter with n-type</td></tr>
</table>

	MOSFET load, CMOS inverter. **Module-VI:**(L –06) **MOS Inverters (Switching Characteristics and Interconnects effects):** Delay-time definitions, calculation of delay times, logical efforts, inverter design with delay constraints, estimation of interconnect parasitics, calculation of interconnect delay, Bus vs. Network-on-Chip (NoC), switching power dissipation of CMOS inverters. **Module-VII:**(L –05) **Combination CMOS Logic Circuits:** MOS logic circuits with depletion nMOS loads, CMOS logic circuits, complex logic circuits, CMOS transmission gates (pass gates), ratioed, dynamic and pass transistor logic circuits. **Module-VIII:**(L –04) **Sequential MOS logic circuits:** Behaviour of bi-stable elements, SR latch circuits, clocked latch and flip-flop circuits, CMOS D-latch and edge-triggered flip-flop. Timing path, Setup time and hold time static, example of setup and hold time static, setup and hold slack, clock skew and jitter, Clock, reset and power distributions. **Module-IX:** (L –04) **Semiconductor Memories:** Memory Design, SRAM, DRAM structure and implementations. **Module-X:**(L –04) **Recent Trends in VLSI Design & its research issues in industry:** System case studies. Design automation of VLSI Systems: basic concepts. Deep Sub-micron Technologies: Some Design Issues.
Text Books, and/or reference material	**Text Book** 1. N. H. E. Weste and C. Harris, "Principles of CMOS VLSI Design: A System Perspective, 3rd Edition, Pearson Education 2007. 2. CMOS Digital Integrated Circuits, Sung-Mo Kang,YusufLeblebici, 3rd edition, Tata McGraw-Hill, 2003 **References:** 1. J. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall 2004.

EC 1013: Digital IC Design (Core)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Acquire idea about the digital IC design techniques.	1	1	2	2	3	2
CO 2	Understand the characteristics of CMOS inverter	1	1	2	2	3	1
CO 3	Learn the basic steps of ASIC Design Flow and fabrication process.	1	1	2	3	3	3
CO 4	Analyze the static and dynamic characteristics of CMOS circuits	2	1	2	3	3	1
C0 5	Design and implementation of combinational and sequential circuits	1	1	2	3	3	2
CO 6	Evaluate the performance of CMOS circuits	1	1	2	3	3	1
Average		**1.17**	**1**	**2**	**2.67**	**3**	**1.67**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC2011</td><td>VLSI Technology</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="2">Semiconductor Device and Modeling (EC1011)</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To study the various processes of IC fabrication</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Outline the basics of semiconductor crystal properties
CO#2: Identify the fundamentals of IC fabrication
CO#3: Illustrate the different methods involved in VLSI fabrication process
CO#4: Appreciate the advanced methods involved in IC fabrication.
CO#5: Build the knowledge of process integration-NMOS, CMOS.</td></tr>
<tr><td>Syllabus/ Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 01)
Introduction: History of IC’s; Operation & Models for Devices of Interest: CMOS and MEMS.

Module-II: (L – 02)
Electronic Materials: Crystal Structures, Defects in Crystals, Si, Poly Si, Si Crystal Growth.

Module-III: (L – 03)
Clean room and Wafer Cleaning: Definition, Need of Clean Room, RCA cleaning of Si.

Module-IV: (L – 05)
Oxidation: Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, Oxidation System

Module-V: (L – 05)
Lithography: Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus, Advanced Lithography: E-beam Lithography, X-ray Lithography, Ion Beam Lithography.

Module-VI: (L – 05)
Diffusion: Pre-Deposition and Drive-in Diffusion Modeling, Dose, 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin’s Curves, Diffusion System.

Module-VII: (L – 05)
Ion Implantation: Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post</td></tr>
</table>

	Implantation Annealing, Ion Channeling, Multi Energy Implantation. **Module-VIII:** (L – 05) **Thin Film Deposition:** Physical Vapor Deposition: Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types, Boundaries and Flow, Different kinds of CVD techniques: APCVD, LPCVD, Metallorganic CVD (MOCVD), Plasma Enhanced CVD etc. **Module-IX:** (L – 02) **Etching:** Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching. **Module-X:** (L – 04) **Metallization/Interconnects:** Overview of Interconnects, Contacts, Metal gate/Poly Gate, Metallization, Problems in Aluminum Metal contacts, Al spike, Electromigration, Metal Silicides, Multi-Level Metallization, Planarization, Inter Metal Dielectric. **Module-XI:** (L – 03) NMOS, CMOS process etc.
Text Books, and/or reference material	**Text Books:** 1. VLSI Technology, S. M. Sze, 2nd Edition, McGraw Hill, 2003. 2. Silicon Process Technology, S K Gandhi,2nd Edition, Wiley India,2009 **References:** 1. Silicon VLSI Technology, Plummer, Deal and Griffin ,1st Edition, Pearson Education,2009 2. Fundamental of Semiconductor Fabrication, Sze and May,2nd Edition, Wiley India,200

EC 2011: VLSI Technology (Core)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Outline the basics of semiconductor crystal properties	1	1	3	2	1	1
CO 2	Identify the fundamentals of IC fabrication	1	1	3	3	2	1
CO 3	Illustrate the different methods involved in VLSI fabrication process	2	2	3	2	3	1
CO 4	Appreciate the advanced methods involved in IC fabrication	2	2	3	3	3	1
CO 5	Build the knowledge of process integration-NMOS, CMOS	3	3	3	3	3	1
Average		**1.8**	**1.8**	**3**	**2.6**	**2.4**	**1**

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours : 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC2012</td><td>VLSI Systems Design</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites:</td><td colspan="6">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="2">Digital and Analog IC/VLSI Design</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To illustrate the basic concepts of modern VLSI circuit design
Describe the fundamental principles underlying digital design using CMOS logic and analyse the performance characteristics of these digital circuits.
Design the synthesizable digital sub-system components using Verilog HDL
Verify that a design meets its functionally, timing constraints, both manually and through the use of computer-aided design tools.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Understand the custom and semi-custom digital IC design flow in VLSI.
CO#2: Understand the concept of logic synthesis, optimization, and scheduling and resource allocation and learn how to apply these to multimillion gate designs.
Co#3: Learn to design a digital system without any timing issues by understanding the Problems associated with such systems like slack, skew, jitter and interconnect noises.
CO#4: Identify and interpret the design towards realizing digital IC design.
CO#5: Design and analyse the performance (speed, power) of CMOS digital integrated circuits for different specifications.</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I:(L – 07)
Design Methodology: Structured design techniques; Programmable logic; Gate array and sea of gates design; cell based design; full custom design; Design flow; Design Economics.

Module-II:(L – 05)
Data path Subsystems: Adders; One/zero Detectors; Comparators; Counters; Shifters; Multipliers; Power and Speed Trade-off.

Module-III:(L – 05)
Memory and Array Subsystems: Memory controller and management, SRAM, DRAM, ROM, Serial access memories; CAM, PLAs; Array yield, reliability; Power dissipation in Memories.

Module-IV:(L – 05)
Special purpose Subsystems: Packaging; power distribution; I/O pads;

Module-V:(L – 05)
Interconnect: Interconnect parameters; Electrical wire models, capacitive parasitics; Resistive parasitics; Inductive parasitic; Crosstalk; Advanced Interconnect Techniques.

Module-VI:(L – 05)</td></tr>
</table>

	Timing Issues: Timing classification; Synchronous design; Self-timed circuit design; **Module-VII:**(L – 08) Clock Synthesis and Synchronization: Synchronizers; Arbiters; Clock Synthesis; PLLs; Clock generation; Clock distribution; Synchronous Vs Asynchronous Design. GPIO, UART, USART, I2C and CAN.
Text / Ref. Books	**Text Books:** 1. Neil H. E. Weste, David. Harris and Ayan Banerjee, "CMOS VLSI Design" - Pearson Education, Third Edition, 2004. 2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits" Pearson Education, Second Edition. **References:** 1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits" TMH, Third Edition, 2003 2. Wayne Wolf, "Modern VLSI Design ", 2nd Edition, Prentice Hall, 1998.

EC 2012: VLSI Systems Design (Core)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 2	PSO 2	PSO 3
CO 1	Understand the custom and semi-custom digital IC design flow in VLSI.	1	1	2	1	1	1
CO 2	Understand the concept of logic synthesis, optimization, and scheduling and resource allocation and learn how to apply these to multimillion gate designs.	2	1	2	3	2	1
CO 3	Learn to design a digital system without any timing issues by understanding the Problems associated with such systems like slack, skew, jitter and interconnect noises.	2	2	3	3	3	1
CO 4	Identify and interpret the design towards realizing digital IC design.	2	2	2	3	3	1
CO 5	Design and analyse the performance (speed, power) of CMOS digital integrated circuits for different specifications.	3	2	3	3	3	1
Average		**2**	**1.6**	**2.4**	**2.6**	**2.4**	**1**

B. Laboratory Courses

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC1061</td><td>Design Laboratory I (Analog IC Design)</td><td>Lab</td><td>0</td><td>0</td><td>4</td><td>4</td><td>2</td></tr>
<tr><td colspan="3">Pre-requisites / Co-requisites
Basic knowledge of Linux and Devices / Circuits</td><td colspan="5">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="3">NIL</td><td colspan="5">CT+EA</td></tr>
<tr><td>Course Objective</td><td colspan="7">To Design and characterize CMOS Analog blocks using CAD tools in Modern CMOS process.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">After going through the course, student will be able to
CO#1: Operate CAD tools (Cadence/Mentor) to simulate Analog blocks in Modern CMOS process.
CO#2: Determine the characteristics of active/ & passive devices for modeling and analysis.
CO#3: Design an inverter (and other basic gates) based on the given specifications.
CO#4: Optimize a Differential amplifier to meet the target specification
CO#5: Appreciate various performance metrics like CMRR, ICMR, PSRR, SR, Power Dissipation, Delay, and Noise Margin with respect to design variables.
CO#6: Examine the effect of process variation using Monte Carlo simulation</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">List of experiments

1. Determination of NMOS and PMOS characteristics
2. Determination of NMOS and PMOS device parameter (V_{T0}, k',λ, γ, SS)
3. Simulation of NMOS and PMOS Resistive Load Inverter.
4. Simulation of CMOS Inverter and measure its delay, Noise margin, power
5. Design of a voltage reference and simple, cascode current mirror
6. Design & simulation of Common Source Amplifier
7. Simulation of Ring Oscillator.
8. Monte Carlo Simulation and process variation</td></tr>
<tr><td>Text/ Reference material</td><td colspan="7">1. Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill
2. Cadence Tutorials : https://nano.wiki.ifi.uio.no/Cadence-Tutorial-English-cadence_6.1.6
3. Cadence Tutorials : https://www.youtube.com/channel/UCEXcqylc45jam5xa6vvEG7A https://www.youtube.com/channel/UCM84pD-OsnS4-O3tTsr8gZA</td></tr>
</table>

EC 1061: Design Laboratory I
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Operate CAD tools (Cadence/Mentor) to simulate Analog blocks in Modern CMOS process.	3	1	2	2	2	1
CO 2	Determine the characteristics of active/ & passive devices for modeling and analysis.	1	1	3	3	3	1
CO 3	Design an inverter (and other basic gates) based on the given specifications.	2	2	3	3	3	1
CO 4	Optimize a Differential amplifier to meet the target specification	3	1	2	2	2	1
CO 5	Appreciate various performance metrics like CMRR, ICMR, PSRR, SR, Power Dissipation, Delay, and Noise Margin with respect to design variables.	1	1	3	3	3	1
CO 6	Examine the effect of process variation using Monte Carlo simulation	3	1	2	2	2	2
Average		**2**	**1.2**	**2.6**	**2.6**	**2.6**	**1**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)#</td><td>Total Hours</td></tr>
<tr><td>EC1062</td><td>Design Laboratory II (Digital IC Design)</td><td>PCR</td><td>0</td><td>0</td><td>4</td><td>4</td><td>2</td></tr>
<tr><td colspan="2">Pre-requisites/Co-requisites</td><td colspan="6">Course Assessment methods (Continuous evaluation (CE) and end assessment (EA))</td></tr>
<tr><td colspan="2">Knowledge of Basic Electronics, Semiconductor Devices, and Digital Electronics,
Analog IC Design (EC1012)</td><td colspan="6">CE+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Acquire the concepts of digital VLSI design
CO2: Understanding of HDL coding and simulation using EDA tools
CO3: Analyze the combinational and sequential circuits
CO4: Design and implementation of combinational and sequential circuits
CO5: Evaluate the performance of digital circuits</td></tr>
<tr><td>Topics Covered</td><td colspan="7">List of experiments

1. Design and Implementation of combinational circuits using data flow or gate level modelling along with their test bench
I. Basic Gates
II. Half-Adder and Full-Adder
III. Half-Subtractor and Full-Subtractor
IV. 2:4 Decoder
V. 8:3 Encoder
VI. Parity Checker
VII. 8:1 Multiplexer
VIII. 1:4 De-multiplexer
IX. Binary to gray converter
X. Gray to binary converter
XI. 2-bit magnitude comparator

2. Design and Implementation of sequential circuits along with their test bench
I. Design and simulation of Flip-flops (RS FF, JK FF, T FF, D FF& Master-slave FF) using VHDL\ Verilog
II. Design and simulation of Counters (Synchronous and Asynchronous) using VHDL\ Verilog.
III. Design and Simulation of Shift registers (SISO, SIPO, PISO & PIPO) using VHDL\ Verilog.
IV. Design an Arithmetic unit using VHDL\ Verilog.

3. Spec. to GDSII using Synopsys tools

<u>Specifications</u>: Two counter – one clocked by an external clock, the other by an internally generated clock. All clocks have to be identified for static timing to work correctly. Total 40 flip-flips nowhere near the limit in terms of area for this chip size. Only four outputs and two inputs, power, and ground. The total is 8 pins</td></tr>
</table>

Text Books, and/or reference material	Suggested Text Books: 1. Samir Palnitkar, Verilog HDL, Second Edition, Pearson education 2003 2. Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill 3. Cadence Design Tutorials in YouTube.

EC 1062: Design Laboratory II
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	**Acquire** the concepts of digital VLSI design	3	1	2	2	2	1
CO 2	**Understanding** of HDL coding and simulation using EDA tools	1	1	3	3	3	1
CO 3	**Analyze** the combinational and sequential circuits	2	2	3	3	3	1
CO 4	**Design** and **implementation** of combinational and sequential circuits	2	2	3	3	3	1
CO 5	**Evaluate** the performance of digital circuits	2	2	3	3	3	1
Average		**2**	**1.6**	**2.8**	**2.8**	**2.8**	**1**

Department of Electronics and Communication Engineering							
Course Code	Title of the course	Program Core (PCR) / Electives (PEL)	Total Number of contact hours				Credit
			Lecture (L)	Tutorial (T)	Practical (P)	Total Hours	
EC2061	**Design Lab III (Mixed Signal IC Design)**	Lab	0	0	4	4	2
Pre-requisites / Co-requisites		Course Assessment methods (Continuous (CT) and end assessment (EA))					
NIL		CT+EA					
Course Objective	This lab introduces CMOS schematic design, layout techniques, automated design tools, netlist synthesis, place & route and timing verification. Entire EDA Tool flow for a Mixed Signal Chip will be introduced in this Lab.						
Course Outcomes	CO#1 Employ CAD tools to carry out Mixed Signal Design using bottom up approach CO#2 Illustrate gm/ID plots and its use in Analog Circuit Design CO#3 Design Opamps to meet any given specification CO#4 Design of a Comparator CO#5 Draw the Layout and compare Pre-layout & Post Layout performance						
Topics Covered/ Syllabus	**List of experiments** : 1. Generation of gm/ID plots for various Channel lengths. 2. Design and simulation of Constant g_m Circuit. 3. Design and optimze a Single stage Opamp 4. Design and optimize a Two stage Opamp 5. Design of Band-gap reference Circuit 6. Design and Simulation of a Comparator / Latch 7. Design of 8 bit Flash ADC and measure its DNL, INL etc. 8. Layout of CMOS a) Inverter and ii) Opamp & Perform post Layout Simulation using Assura/Calibre						
Reference materials	1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill Education, 2002. 2. Allan Hastings, The Art of Analog Layout, Prentice Hall, Second Edition, 2005.						

EC 2061: Design Laboratory III
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Employ CAD tools to carry out Mixed Signal Design using bottom up approach	1	1	2	3	3	1
CO 2	Illustrate gm/ID plots and its use in Analog Circuit Design	2	2	2	3	3	1
CO 3	Design Opamps to meet any given specification	2	2	2	3	3	1
CO 4	Design of a Comparator	3	2	3	3	3	1
CO 5	Draw the Layout and compare Pre-layout & Post Layout performance	3	3	3	3	3	2
Average		**2.2**	**2**	**2.4**	**3**	**3**	**1.2**

C. Elective Courses

<table>
<tr><th colspan="8">Department of Electronics and Communication Engineering</th></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours : 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9039</td><td>CAD for VLSI</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites:</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">Digital Design and Programming Language</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Extend knowledge of CAD tools, Verilog and their applications in Xilinx to verify the circuit functionality in digital domain.
CO#2: Introduce students to the concepts and use of Verilog in the Xilinx to a digital system.
CO#3: Provide sufficient knowledge and experience so that students will be able to make meaningful design choices when asked to design any digital circuit to meet or exceed design specifications.</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 03)
Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, Verilog HDL, Trends in HDLs.

Module-II:(L – 03)
Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

Module-III:(L – 03)
Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.Memory modelling Logic Synthesis: Introduction synthesis of different Verilog constructs.

Module-IV:(L –03)
Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing.Introduction to Reconfigurable computing, FPGAs, the Altera /Xilinx flow.

Module-V:(L – 02)</td></tr>
</table>

	Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. **Module-VI:**(L – 03) **Dataflow Modeling:** Continuous assignments, delay specification, expressions, operators, operands, operator types. **Module-VII:**(L – 03) **Behavioural Modeling:** Structured procedures, initial and always, blocking and nonblocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks. **Module-VIII:**(L – 04) **Tasks and Functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions. **Module-IX:**(L – 04) **Useful Modeling Techniques:** Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks. **Module-X:**(L – 04) **Flip-Flop and Counter Design:** Synchronous and asynchronous flip flop design with set and reset, design of basic counters. **Module-XI:**(L – 04) Introduction to FPGAs **Module-X:** (L – 04) Essential System Verilog for UVM: Overview of basic SystemVerilog, UVM verification environment: introduction to UVM methodology and universal Verification Components (UVC) structure, stimulus modeling, creating a simple environment, DUT, TLM, functional coverage modeling, register modeling in UVM.
Text / Ref. Books	**Text Books:** 1. Verilog HDL, Samir Palnitkar, Second Edition, Pearson Education, 2004 2. Verilog HDL Synthesis, J. Bhaskar, BS publications, 2001. **Reference:** 1. Fundamentals of Digital Logic with Verilog Design, Brown & Vranesic, McGraw-Hill Companies, Incorporated, 2007.

EC 9039: CAD for VLSI (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Extend knowledge of CAD tools, Verilog and their applications in Xilinx to verify the circuit functionality in digital domain.	1	1	3	2	2	1
CO 2	Introduce students to the concepts and use of Verilog in the Xilinx to a digital system.	2	1	3	2	2	1
CO 3	Provide sufficient knowledge and experience so that students will be able to make meaningful design choices when asked to design any digital circuit to meet or exceed design specifications.	3	2	3	3	3	1
Average		**2**	**1.33**	**3**	**2.33**	**2.33**	**1**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC 9034</td><td>Digital Signal Processing and Applications</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">Signals and Systems (ECC303), Mathematics-II & III (MAC MAC331)</td><td colspan="6">Class Assignments, Quiz, Mid and End Term examinations</td></tr>
<tr><td>Course Objective</td><td colspan="7">The course teaches Introduction to DSP; Digital Systems – Characterization, Description and Testing; FIR and IIR: Recursive and Non Recursive; Discrete Fourier Transform; Z Transform; Discrete Time Systems in Frequency Domain; Simple Digital Filters; Digital Processing of Continuous Time Signals; Analog Filter Design; Digital Filter Structure, Synthesis and Design</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Analyse a given signal or system using tools such as Fourier transform and z-transform to know the property of a signal or system.
CO#2: Process signals to make them more useful; and how to design a signal processor for a given problem, construct simple IIR and FIR filter.
CO#3: Design and Analysis of various types of Analog Butterworth and Chebyshev filters.
CO#4: Design methods to convert analog filters into digital filters.
CO#5. Perform Frequency transformations in Analog and Digital domains. Realization of Digital FIR and IIR Filter Structure.</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">Total Lecture hours: 40

Module-I:(L – 02)
Introduction: reasons behind digital processing of signals, brief historical development, organization of the course.

Module-II:(L – 05)
Theory of discrete time linear system sequences, linear time invariant systems, causality, stability, difference equations, frequency response, discrete Fourier series, relation between continuous and discrete systems, Inverse Systems, Stability.

Module-III:(L – 05)
Z –transform: definition, properties of Z transform, system function, digital filter implementation from the system function, region of convergence in the Z plane, determining filter coefficients from the singularity locations, geometric evolution of Z transform in the Z plane, relationship between Fourier transform and Z transform, inverse Z transform.

Module-IV:(L – 05)
Transform technique: Fourier transform, its properties, inverse Fourier transform, discrete Fourier transform, properties of DFT, circular convolution, computations for evaluating the DFT, decimation in time and decimation in frequency FFT algorithms, discrete Hilbert transform.

Module-V:(L – 04)
Digital filter structures: system describing equations, filter categories, All Pass Filters, Comb Filters, direct form I and II structures, cascade and parallel communication of second order systems, Polyphase representation of filters, linear phase FIR filter structures, Compensatory Transfer Functions, frequency sampling structure for the FIR filter. Test for</td></tr>
</table>

	Stability using All Pass Functions. **Module-VI:**(L – 05) IIR filter design techniques: Analog Filter Design, Analog Butterworth lowpass filter design techniques, Analog Chebyshev LPF, Design methods to convert analog filters into digital filters, frequency transformation for converting lowpass filters into other types, all-pass filters for phase response compensation. **Module-VII:**(L – 05) Digital Filter Structures: IIR Realizations, All Pass Realizations, FIR and IIR Lattice Synthesis, IIR Design by Bilinear Transformation, Digital to Digital Frequency Transformation. **Module-VIII:**(L – 05) FIR filter design techniques: Windowing method for designing FIR filters, DFT method for approximating the desired unit sample response, combining DFT and window method for designing FIR filter, frequency sampling method for designing FIR filter. **Module-IX:**(L – 04) Non-Linear System Identification Schemes, Fractional-order digital differentiators (DDs) and digital integrators (DIs), Fractional-order low-pass Butterworth and Chebyshev filter.
Text Books, and/or Reference material	Text Books: 1) Discrete-Time Signal Processing (Second Edition), Alan V. Oppenheim, Ronald W. Schafer, and John R. Buck, Pearson Education India 2) Digital Signal Processing: Principles, Algorithms and Applications (3rd Edition), John G. Proakis, Dimitris G. Manolakis, and D Sharma, Pearson Education India 3) Richard G. Lyons, Understanding Digital Signal Processing, Prentice Hall, 1996. 4) Digital Signal Processing by Tarun Kumar Rawat, Oxford University Press.
	Reference Books/materials: 1) S. W. Smith, The Scientist and Engineer's and Guide to Digital Signal Processing, California Technical Publishing, 1997. ISBN: 0-9660176-3. 2) Digital Signal Processing using MATLAB, Vinay K. Ingle, John G. Proakis, Brooks/Cole-Thomson Learning

EC 9034: Digital Signal Processing & Applications (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Analyse a given signal or system using tools such as Fourier transform and z-transform to know the property of a signal or system.	3	2	1	3	2	1
CO 2	Process signals to make them more useful; and how to design a signal processor for a given problem, construct simple IIR and FIR filter.	1	2	1	1	1	1
CO 3	Design and Analysis of various types of Analog Butterworth and Chebyshev filters.	3	3	3	3	2	2
CO 4	Design methods to convert analog filters into digital filters.	3	3	3	2	2	2
CO 5	Perform Frequency transformations in Analog and Digital domains. Realization of Digital FIR and IIR Filter Structure.	3	3	2	3	3	3
Average		**2.6**	**2.6**	**2**	**2.4**	**2**	**1.8**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9041</td><td>Mixed Signal IC Design</td><td>PEL (Elective)</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites / Co-requisites</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">NIL</td><td colspan="6">Class Assignments, Quiz, Mid and End Term examinations</td></tr>
<tr><td>Course Objective</td><td colspan="7">To introduce the fundamental concepts of mixed-signal circuit design;</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Analyze and differential amplifiers
CO#2: Understand the design methodology for mixed signal IC design using gm/Id concept.
CO#3: Understand various compensation schemes used in opamp
CO#4: Design the CMOS opamp and based on given specification
CO#5: Appreciate the fundamentals of data converters and also optimized their performances
CO#6: Able to design mixed-signal building blocks like comparators and PLL.</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 04)
High performance CMOS operational transconductance amplifiers analysis. Operation of fully differential amplifiers, Types of common mode feedback circuits, Gilbert Cell.

Module-II: (L – 05)
Introduction to gm/Id technique and Design method using gm/Id technique. Generation of gm/ID, gm/gds, ft plots using CAD tools. Design of amplifiers using gm/Id technique.

Module-III: (L – 05)
Frequency compensation schemes: Dominant-Pole Compensation, Shunt-Capacitance Compensation, Miller Compensation, Pole-Zero Compensation, Feed-forward Compensation.

Module-IV: (L – 06)
Switched capacitor circuits, design of switched capacitor amplifiers and integrators, effect of opamp finite gain, bandwidth and offset, circuit techniques for reducing effects of opamp imperfections, switches and charge injection and clock feed-through effects.

Module-V: (L – 06)
Design of sample and holds and comparators.

Module-VI: (L – 06)
Fundamentals of data converters; Nyquist rate A/D converters (Flash, interpolating, folding flash, SAR and pipelined architectures); Nyquist rate D/A converters - voltage, current and charge mode converters; Oversampled A/D and D/A converters.

Module-VII: (L – 08)
Basic PLL topology, dynamics of simple PLL, phase detectors, Phase frequency detector, Loop filters, Charge Pump PLLs, Ring Oscillator, VCO.</td></tr>
</table>

Text Books, and/or Reference material	Text Books: 4. Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill 1. R. Gregorian - Introduction to CMOS Opamps and Comparators. Wiley
	Reference: 1. T. Carusone, D. Johns and K. Martin - Analog integrated circuit Design

EC 9041: Mixed Signal IC Design (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Analyze and differential amplifiers.	2	1	3	1	1	1
CO 2	Understand the design methodology for mixed signal IC design using gm/Id concept.	1	1	3	2	1	1
CO 3	Understand various compensation schemes used in opamp.	1	1	3	2	1	1
CO 4	Design the CMOS opamp and based on given specification.	2	2	3	3	2	1
CO 5	Appreciate the fundamentals of data converters and also optimized their performances.	2	2	3	2	2	1
CO 6	Able to design mixed-signal building blocks like comparators and PLL.	3	3	3	2	3	1
Average		**1.83**	**1.67**	**3**	**2**	**1.67**	**1**

<table>
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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9042</td><td>Low Power Circuits and Systems</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites:</td><td colspan="6">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="2">EC1013: Digital and Analog IC Design.</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">The course deals with issues and models to design low-power VLSI circuits and systems, covering fundamentals of power dissipation, leakage mechanisms and various low power techniques in a CMOS digital circuit.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Acquire knowledge of the fundamentals and applications of Low-power circuits.
CO#2: Identify various leakage/ switching power sources in a MOSFET and a digital circuits.
CO#3: Analyze the various issues to power dissipation and techniques to minimize/optimize
CO#4: Learn various leakage/ switching power reduction mechanisms at device level and circuit level.
CO#5: Design and implementation of a power-aware circuits and systems.
CO#6: Evaluate the performance of low power circuits and systems</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I:(L – 05)
Introduction: Need for Low power VLSI chips - Low Power Design Methodology - Logic synthesis for Low power.

Module- II: (L- 04)
Sources of power dissipation in CMOS circuits: static power dissipation-diode leakage power, sub-threshold leakage power, gate and other tunnel currents; dynamic power dissipation - short circuit power, switching power, Glitching power; degrees of freedom.

Module-III: (L – 07)
Power Analysis and Estimation: Gate level Analysis, Architecture level Analysis, Data Correlation Analysis, Monte-Carlo Simulation, Probabilistic Power Analysis. Statistical Techniques - Estimation of Glitching Power - Sensitivity Analysis - Circuit Reliability - Power Estimation at the circuit level - High level Power Estimation - Estimation of maximum power.

Module-IV: (L – 08)
Static Power Optimization Techniques: Leakage current in deep sub micrometer transistors- Transistor Leakage Mechanism, Leakage Current Estimation. Multiple threshold voltages, various approaches for the fabrication of multiple threshold voltage transistors, variable threshold voltage CMOS (VTCMOS), transistor tracking approach, run time leakage power- multiple-threshold voltage (MTCMOS), power gating technique and various issues related to power gating approaches, state retention strategy,</td></tr>
</table>

	power management techniques, dual-V_t technique, delay and energy constrained dual-V_t techniques. **Module-IV:** (L – 08) Dynamic Power Optimization Techniques: Supply voltage scaling approaches: parallelism, pipelining, using multiple supply voltage, module level voltage selection, clustered voltage scaling, level converters, multiple supplies inside a block, supply voltage limitations, Optimum supply voltage, multi-level voltage scaling (MVS), dynamic voltage and frequency scaling (DVFS), adaptive voltage scaling (AVS), System level approach- hardware/software co-design, encoding techniques, clock gating, gated clock finite state machines (FSMs), pre-computational logic, basic approach of minimizing glitching power, Dynamic CMOS and Pass-transistor logic styles. **Module-V:** (L – 04) Low Power Static RAM Architectures: Organization, MOS Static RAM Memory Cell, Banked Organization, Voltage Swing Reduction, Power Reduction. **Module-VI:** (L – 04) Low Voltage CMOS VLSI Technology: BICMOS and Silicon On Insulator (SOI) Technology. Recent Trends in low power VLSI Designs & its research issues in industry.
Text / Ref. Books	**Text Books:** 1. Anantha P Chandrakasan and Robert W Brodersen, "Low Power Digital CMOS Design", Kluwer Academic Publishers, Holland, 1995. 2. Ajit Pal, "Low Power VLSI Circuits and Systems", Springer, 2015. **References:** 1. Gary B Yeap K, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998. 2. Kuo J B and Lou J H, "Low Voltage CMOS VLSI Circuits", John Wiley and Sons, Singapore, 1999. 3. Kaushik Roy and Sharat C Prasad, "Low Power CMOS VLSI circuit Design", John Wiley and Sons, 2000.

EC 9042: Low Power Circuits and Systems (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	**Acquire** knowledge of the fundamentals and applications of Low-power circuits	2	1	2	2	1	1
CO 2	**Identify** various leakage/ switching power sources in a MOSFET and a digital circuits.	3	1	3	3	3	1
CO 3	**Analyze the v**arious issues to power dissipation and techniques to minimize/optimize	3	2	3	3	3	1
CO 4	**Learn** various leakage/ switching power reduction mechanisms at device level and circuit level.	3	2	3	2	2	1
CO 5	**Design and implementation** of a power-aware circuits and systems	2	1	2	3	3	2
CO 6	**Evaluate** the performance of low power circuits and systems	2	1	2	3	3	2
Average		**2.50**	**1.33**	**2.50**	**2.67**	**2.50**	**1.33**

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<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9044</td><td>RF IC Design</td><td>PEL
(Open Elective)</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites / Co-requisites</td><td colspan="5">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="3">Communication Theory, Signals and Systems, Analog IC Design</td><td colspan="5">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objective</td><td colspan="7">The objective of the course is to give the student fundamental knowledge on Radio Frequency (RF) integrated circuits design. The course discusses methods and techniques for RF front-end design oriented to CMOS technology.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Analyze various architectures of today’s digital radio transmitters and receivers
CO#2: Analyze and design basic RF building-blocks in CMOS technology
CO#3: Verify and optimize RF blocks (circuits) using a professional software
CO#4: Define basic RF measurements parameters such as S-parameters, sensitivity, noise figure, IIP3
CO#5:Appreciate the different LNA topologies & design techniques</td></tr>
<tr><td>Topics Covered/ Syllabus</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 06)
Basic Concepts in RF Design, Architectures, Transmission media and Reflections, Maximum power transfer, Scattering Parameters

Module-II: (L – 06)
Modern IC technologies (CMOS, Si-Ge, SoI), fundamental limitation of speed & gain of transistors in various technologies

Module-III: (L – 06)
Different Noise Mechanisms: Classical two-port noise theory, noise models for active and passive components

Module-IV: (L – 06)
Low Noise Amplifiers: SNR, LNA topologies, power constrained noise optimization, linearity and large signal performance. Linearity consderations,1-dB compression, IIP, THD estimation.

Module-V: (L – 04)
Passive and Active Mixers: multiplier-based mixers, sub-sampling mixers, diode-ring mixers.

Module-VI: (L – 04)
RF Passive Components: Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines.

Module-VII: (L – 04)
Oscillators: Basic Principles, Cross-Coupled VCO, Phase Noise

Module-VIII: (L – 04)
RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power</td></tr>
</table>

	amplifiers, linearity considerations.
Text Books, and/or Reference material	Text Books: 1. RF Microelectronics, Behzad Razavi, Prentice Hall of India (2001) 2. VLSI for Wireless Communication, Bosco Leung, Springer (2011)
	Reference: 1. Thomas H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press.

EC 9044: RF IC Design (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Analyze various architectures of today's digital radio transmitters and receivers	2	1	2	2	1	1
CO 2	Describe various basic RF building-blocks in CMOS technology	3	1	3	3	3	1
CO 3	Choose and optimize RF blocks (circuits) using CAD tools	3	2	3	3	3	1
CO 4	Define basic RF measurements parameters such as S-parameters, sensitivity, noise figure, IIP3	3	2	3	2	2	1
CO 5	Select appropriate LNA/Mixer/Oscillator topologies & design them	2	1	2	3	3	2
Average		**2.50**	**1.33**	**2.50**	**2.67**	**2.50**	**1.33**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9046</td><td>FPGA based Design</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">Boolean algebra, Logic design fundamentals</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Explain logic synthesis techniques – two level and multilevel synthesis.
CO2: Design systems using FPGAs and CPLDs.
CO3: Design sequential machine design using FPGAs.
CO4: Design systems for low power operation.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 05)
Logic design fundamentals: Two level synthesis – SOP/POS forms, Logic minimization, Limitations of two level synthesis, introduction to multi-level synthesis.

Module-II: (L – 05)
Programmable Logic Devices: Programmable Logic Array (PLA) architecture; Programmable Array Logic (PAL), PAL vs. PROM, Fan-in expansion feature, Architecture for sequential circuit implementation, Typical PAL chips; Complex Programmable Logic Devices (CPLD).

Module-III: (L – 07)
Programmable Gate Arrays: Gate Array concept, Mask programmable and Field Programmable Gate Arrays; Look up tables (LUT) Configurable logic blocks (CLB), logic design using LUT’s; Multi-level synthesis techniques – Factoring and Functional decomposition, Shannon’s Expansion Theorem; Generalized FPGA Architecture.

Module-IV: (L – 06)
Sequential Circuit Design: Finite State Machines, Moore and Mealy Machines; State diagrams, State table, State assignment, derivation of next-state and output expressions, state minimization; State assignment for low power operation; CAD tools for FSM synthesis.

Module-V: (L – 04)
Advanced features of modern FPGAs: Block RAMs, Embedded processor, Communication ports, Analog interface.

Module-VI: (L – 06)
Typical case studies: Simple logic functions – Decoder, encoder, multiplexer, demultiplexer, BCD to seven-segment decoder, keyboard/display interface; memory elements and arrays; sequential machine design – sequence generators, timing generators, a typical machine design (example: vending machine); A simple CPU design.

Module-VII: (L – 04)
Design analysis: Static timing analysis, Power analysis, Resource utilization, noise, clock network, DRC, debugging methods.

Module-VIII: (L – 04)
FPGA as a Hardware Debugging platform: Hardware troubleshooting methods, Looking into the chip – Logic State Analyzer and its use; Concept of Hardware emulation – simulation vs. Emulation, FPGA as a Hardware emulator, Break-points and their utility,</td></tr>
</table>

	setting break-points in FPGA based design.
Text Books, and/or reference material	Text Books: 1. Fundamentals of Digital Logic with Verilog Design by S. Brown and Z. Vranesic (McGraw Hill.) Reference Books: 1. A Verilog HDL Primer by J. Bhasker (B.S. Publications)

EC 9046: FPGA Based Design (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Learn logic synthesis techniques – two level and multilevel synthesis.	2	1	2	2	1	1
CO 2	Be able to design systems using FPGAs and CPLDs.	3	1	3	3	3	1
CO 3	Learn sequential machine design using FPGAs.	3	2	3	3	3	1
CO 4	Learn to design systems for low power operation.	3	2	3	2	2	1
Average		**2.75**	**1.5**	**2.75**	**2.5**	**2.25**	**1**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9047</td><td>MEMS & Microsystems Technology</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="2">NIL</td><td colspan="6">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">Develop fundamental concepts of MEMS system, MEMS device modeling techniques and learn MEMS device fabrication process and MEMS device packaging</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Understand characteristics of MEMS system
CO#2: Understand basic building blocks of general MEMS systems
CO#3: Apply qualitative and quantitative analysis techniques in general MEMS systems
CO#4: Design techniques in MEMS
CO#5: Investigate complex designs in MEMS systems
CO#6: Understand synthesis and fabrication of MEMS system</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-1: (L – 06)
MEMS device fabrication process

Module-2: (L – 07)
Lumped Modeling, Statics, Dynamics, Quasi static analysis, Energy Methods

Module-3: (L – 06)
Elasticity, Structures, Thermal Energy Domain, Fluids, Electronics

Module-4:(L – 07)
Effect of noise, Feedback systems

Module-5:(L – 07)
Integration of MEMS systems, Scaling effect, Reliability of MEMS devices

Module-6:(L – 07)
Case studies in MEMS.</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
1. Microsystem Design by Stephen D. Senturia, Springer
Reference Books:
1. Micro and Smart Systemsby K.J. Vinoy, S. Gopalakrishnan, K.N. Bhat, V.K. Aatre G.K. Ananthasuresh, Wiley</td></tr>
</table>

EC 9047: MEMS and Microsystems Technology (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	**Understand** characteristics of MEMS system	2	1	3	1	1	1
CO 2	**Understand** basic building blocks of general MEMS systems	1	1	3	2	1	1
CO 3	**Apply qualitative and quantitative analysis** techniques in general MEMS systems	1	1	3	2	1	1
CO 4	**Design** techniques in MEMS	2	2	3	3	2	1
CO 5	**Investigate complex designs** in MEMS systems	2	2	3	2	2	1
CO 6	**Understand** synthesis and fabrication of MEMS system	3	3	3	2	3	1
Average		**1.83**	**1.67**	**3**	**2**	**1.67**	**1**

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9049</td><td>Nanoelectronics</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods (Continuous (CT) and end assessment (EA))</td></tr>
<tr><td colspan="3">Microelectronics and Semiconductor Device Physics (Solid State Devices)</td><td colspan="5">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To present the state of art in the areas of semiconductor device physics and materials technology to enable the Nano-Electronics.
To study the fundamentals of standard CMOS technology and the issue in scaling MOSFET in the sub-100nm regime will be elaborated.
Emerging studies for need of non-classical transistors with new device structure and nanomaterials will be elucidated.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Demonstrate understanding of fundamental of nanodevices fabrication techniques
CO#2: Demonstrate understanding of nanotechnology concepts for device fabrication and characterization.
CO#3: To quire fundamental understanding for electronics and optical properties of nanomaterials.
CO#4: To acquire knowledge of basic nanodevice principles and fabrication approaches for various nanoscale devices.</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 10)
Introduction to nanotechnology, the size of things, history of nanotechnology, fabrication method (top-down and bottom-up), emerging applications of nanotechnology.

Module-II: (L – 10)
Electronic and Optical properties of nanostructures. Energy sub-bands. Electron transport in two –dimensional electron gas (density of states), Carrier scattering, resistance of a ballistic conductor, Transmission probability calculation, Electron tunneling, Resonant tunneling, Coupled nanoscale structures, and Superlattices,

Module-III: (L – 10)
Nanotechnology: Deposition techniques for Nanoscale Devices, Nanolithography, Self-Assembly Techniques, Nanomaterials, Nanoparticles, Nanowires, Nanomagnetic Materials, Nanostructure Surfaces; Instrumentation for nanoscale electronics: The</td></tr>
</table>

	Atomic Force Microscope (AFM), Scanning Tunneling Microscope and scanning near field optical microscope. **Module-IV:** (L – 10) Shrink-down approaches: Electronic devices Based on Nanostructures: Advance Heterostructure Devices, Downscaling of the MOSFET. Nanoscale FET Transistors, the Ballistic FET, Resonant Tunneling Devices and Circuits, Single Electron Transistor and Related Devices. Devices based on carbon nanotubes, Spintronic Devices; Optoelectronic Devices using Nanostructures: Quantum well and Quantum Dot LASERS, Quantum Cascade LASER, Quantum well-infrared photodetector, Superlattice LASER.
Text / Ref. Books	**Text Books:** 1. Introduction to Nanotechnology, C.P. Poole Jr., F.J. Owens, Wiley (2003). 2. Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Waser Ranier, Wiley-VCH (2003). **References:** 1. Nanosystems, K.E. Drexler, Wiley (1992) 2. The Physics of Low-Dimensional Semiconductors, John H. Davies, Cambridge University Press, 1998. 3. Fundamentals of Modern VLSI Devices, Y. Taur and T. Ning, Cambridge University Press. 4. Karl Goser, "Nanoelectronics and Nanosystems," Springer, 2004

EC 9049: Nanoelectronics (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Demonstrate understanding of fundamental of nanodevices fabrication techniques	2	1	2	2	1	1
CO 2	Demonstrate understanding of nanotechnology concepts for device fabrication and characterization.	3	1	3	3	3	1
CO 3	To quire fundamental understanding for electronics and optical properties of nanomaterials.	3	2	3	3	3	1
CO 4	To acquire knowledge of basic nanodevice principles and fabrication approaches for various nanoscale devices.	3	2	3	2	2	1
Average		**2.75**	**1.5**	**2.75**	**2.5**	**2.25**	**1**

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<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9051</td><td>Testing and Verification of VLSI Circuits</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods: (Continuous (CT), Mid-semester assessment (MA) and end assessment (EA)):</td></tr>
<tr><td colspan="3">Digital Design.</td><td colspan="5">Assignments, Quiz, Mid-semester Examination and End Semester Examination</td></tr>
<tr><td>Course Objectives</td><td colspan="7">To expose the students, the basics of testing and verification techniques for the digital IC design.</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Extend knowledge of the requirement of fault modeling in VLSI circuits.
CO#2: Generate test vectors to test a circuit efficiently covering maximum faults.
CO#3: Demonstrate the concept of Memory testing techniques.
CO#4: Discuss about Built-in-Self Test and its application in modern digital design
CO#5: Use modern tools for testing and verification.</td></tr>
<tr><td>Syllabus/Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 05)
Physicalfaultsandtheirmodeling.Faultequivalenceanddominance;fault collapsing, Fault simulation: parallel, deductive and concurrent techniques; critical pathtracing.

Module-II: (L – 05)
Test generation for combinational circuits: Boolean difference,D-algorithm, Podem, random etc. Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.

Module-III: (L – 05)
PLA testing: cross-point fault model, test generation, easily testable designs.

Module-IV: (L – 05)
Memory testing: permanent, intermittent and pattern-sensitive faults; test generation.

Module-V: (L – 05)
Delay faults and hazards; test pattern generation techniques, ATPG and its different types.

Module-VI: (L – 05)
Test pattern generation for sequential circuits: ad-hoc and structures techniques scan path and LSSD, boundary scan.</td></tr>
</table>

	Module-VII:(L – 05) Built-in self-test techniques: LBIST and MBIST. Verification: logic level (combinational and sequential circuits), RTL-level (data path and control path). Verification of embedded systems. Use of formal techniques: decision diagrams, logic-based approaches. **Module-VIII:** (L – 05) ASIC/IP Verification, direct and random testing, Error detection and correction codes.
Text / Ref. Books	**Text Books:** 1. Essentials of Electronic Testing, M. L. Bushnell and V. D. Agrawal,3rd Kluwer Academic Publishers 2002 **References:** 1. Delay Fault Testing for VLSI Circuits,A. Krstic and K-T Cheng,3rd Kluwer Academic Publishers. 2003 2. Testing of Digital Systems, N. K. Jha and S. Gupta, 2nd, Cambridge University Press. 2003 3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, 3rd, Wiley-IEEE Press. 1994 4. Fault Tolerant and Fault Testable P. K. Lala, 4th, Hardware Design, Prentice-Hall. 1986

EC 9051: Testing and Verification of VLSI Circuits (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Extend knowledge of the requirement of fault modeling in VLSI circuits.	1	1	1	2	1	1
CO 2	Generate test vectors to test a circuit efficiently covering maximum faults.	2	2	3	2	1	1
CO 3	Introduce students to the concepts Memory testing techniques.	2	2	2	3	2	1
CO 4	Understanding Built-in-Self Test and its application in modern digital design	2	2	3	2	2	1
CO 5	Use modern tools for testing and verification.	2	2	3	3	2	2
Average		**1.8**	**1.8**	**2.4**	**2.4**	**1.6**	**1.2**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9030</td><td>Artificial Intelligence and Soft Computing</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="6">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="2">NIL</td><td colspan="6">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Basics of optimization and soft computing algorithms
CO2: Learn different soft computing algorithms
CO3: Learn artificial neural network and its training
CO4: Study of radial basis function neural and its training
CO5: Study of machine learning algorithms and clustering</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 07)
Introduction to optimization, Constrained and unconstrained optimization Introduction to Optimization based on soft computing ,Genetic algorithms, Quantum particle swarm optimization, Whale optimization, Crow search algorithm

Module-II: (L – 07)
Flower pollination algorithm,Teaching learning based optimization, Sine cosine algorithm, Moth flame optimization

Module-III: (L – 06)
Backtracking search optimization Algorithm, Particle swarm optimization, Firefly algorithm

Module-IV: (L – 07)
Introduction to artificial neural network,Supervised Learning Neural Networks, Perceptrons, Adaline, Multilayer feed forward neural network, Training of neural network using back propagation algorithm,Training of neural network using soft computing technique

Module-V: (L – 07)
Radial Basis Function Neural Networks(RBF),Training of RBF using pseudo inverse technique, Data clustering using K-means

Module-VI: (L – 06)
Extreme learning machine(ELM),Kernel based ELM, Random vector functional link neural network(RVFL),Training and testing of ELM and RVFL,CNN</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
1.Principles of Soft Computing, S N Sivanandam, S. Sumathi, John Wiley & Sons
2.A beginners approach to Soft Computing, Samir Roy &Udit Chakraborty, Pearson
3. Neural Networks: A Classroom Approach,1/e by Kumar Satish, McGraw Hill
Reference Books:
1.S. Rajasekaran and G.A.V.Pai, Neural Networks, Fuzzy Logic and Genetic Algorithms, PHI
2.Neuro-Fuzzy and Soft computing, Jang, Sun, Mizutani, PHI
3. Neural Networks: A Comprehensive Foundation (2nd Edition), Simon Haykin, Prentice Hall.</td></tr>
</table>

EC 9030: Artificial Intelligence and Soft Computing (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Basics of optimization and soft computing algorithms.	1	1	1	2	1	1
CO 2	Learn different soft computing algorithms.	2	2	3	2	1	1
CO 3	Learn artificial neural network and its training.	2	2	2	3	2	1
CO 4	Study of radial basis function neural and its training.	2	2	3	2	2	1
CO 5	Study of machine learning algorithms and clustering.	2	2	3	3	2	2
Average		**1.8**	**1.8**	**2.4**	**2.4**	**1.6**	**1.2**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC 9013</td><td>Optical Communication</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites:</td><td colspan="6">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="2">Electronic Devices and Circuits, Electromagnetic fields Theory, Analog and Digital Communication</td><td colspan="6">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Students will be able to learn the intricacies of design constraints at optical frequency.
CO2: The basic training for understanding circuits and system level implementation in light wave technology.
CO3: The students can design components and choose appropriate sources and receivers for an optical network.
CO4: Understanding the usage of OTDR in monitoring an optical communication system.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module-I: (L – 02)
Introduction to optical communication: Overview of general communication, advantages of optical communication; Shannon noiseless coding theorem and Shannon noisy coding theorem.

Module-II: (L – 08)
Optical Fiber: Classification of Fibers, Fiber materials and fabrication methods, Ray optics representation and wave optics representation for step index and graded index fibers, Modes, Phase and group velocity, Power flow in step index fibers.

Module-III: (L – 06)
Propagation Characteristics in Optical Fibers: signal attenuation in fiber, dispersion, classification and effect of dispersion in information transfer, review of fiber connectors, couplers, optical filter, isolator, circulator and attenuator.

Module-IV: (L – 08)
Design aspects of optical communication: optical fiber systems, modulation schemes, digital and analog fiber communication system, system design consideration, emitter and detector design, fiber choice, connectors, various amplifiers and its characteristics; OTDR

Module-V: (L – 02)
Optical transmitter: Basic concepts, characteristics of semiconductor injection LASER, LED, transmitter design

Module-VI: (L – 06)
Optical Receiver: Basic concepts, p-n and p-i-n photo detectors, Avalanche photo detectors, MSM photo detector, receiver design, receiver noise, receiver sensitivity, optical amplifier and its applications; Direct detection; Coherent communication: Basic concept, detection principles, practical considerations, modulation and demodulation schemes, heterodyne and homodyne detection, single and multicarrier systems, DPSK system.

Module-VII: (L – 04)</td></tr>
</table>

	Wavelength division multiplexing (WDM): multiplexing techniques, topologies and architectures, wavelength shifting, WDM demultiplexer, optical add/drop multiplexers. **Module-VIII:** (L – 04) **Dense wavelength division multiplexing (DWDM):** system considerations, multiplexers and demultiplexers; Fiber amplifier for DWDM, SONET/SDH transmission, modulation formats, NRZ and RZ signaling, DPSK system modeling. Potential applications and future prospects of optical fibers, multimode intensity sensors and single mode, Interferometric sensors. Recent trends in optical communication.
Text Books, and/or reference material	**Text Books:** [1] J. M. Senior, "Optical Fiber Communications", PHI, 2nd Ed. [2] G. Keiser, "Optical Fiber Communication", McGraw Hill, 3rd Ed. [3] Ghatak &Thyagarajan, "Introduction to fiber Optics", Cambridge University press. [4] Henry Zanger and Cynthia Zanger, *Fiber Optics Communication and Other Application*, Macmillan Publishing Company, Singapore 1991. **Reference Books:** [1] J.H. Franz & V.K.Jain, "Optical Communications", Narosa Publishing House. [2] Ghatak & Thyagarajan, "Contemporary Optics", Series Title: Optical Physics and Engineering, Springer [3] Amnon Yariv and Pochi Yeh, Photonics: Optical electronics for Modern Communication, 6th Ed., New York, Oxford University Press

EC 9013: Optical Communication
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	**PO2**	**PO3**	**PSO1**	**PSO2**	**PSO3**
CO1	Students will be able to learn the intricacies of design constraints at optical frequency.	**1**	**1**	**2**	**2**	**3**	**1**
CO2	The basic training for understanding circuits and system level implementation in lightwave technology.	**3**	**2**	**3**	**2**	**1**	**2**
CO3	The students can design components and choose appropriate sources and receivers for an optical network.	**2**	**1**	**3**	**1**	**2**	**1**
CO4	Understanding the usage of OTDR in monitoring an optical communication system.	**2**	**2**	**3**	**2**	**2**	**2**

<table>
<tr><td colspan="7">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 43</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC 9014</td><td>Queuing Theory for Telecommunication</td><td>PEL (Program Elective)</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="2">Pre-requisites</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="2">Communication Networks, Engineering Mathematics</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="6">CO#1: Identify standard queuing networks.
CO#2: Integrate transportation and material handling topics with the general queuing models.
CO#3: Analyze case studies to indicate breadth and depth of queuing systems and their range of applicability.
CO#4: Interpret software programs for demonstration and solution of topological network design.</td></tr>
<tr><td>Topics Covered</td><td colspan="6">Total Lecture hours: 43

Module I: (L- 04)
Problem Overview: Introduction to stochastic process, Evolution of queuing and queuing network models and their optimization for traffic congestion and performance.

Module II: (L- 06)
Mathematical Models and Properties of Queues: Modelling of infinite and finite buffer queuing networks especially analysing four categories of queuing networks (Product Form, Non-Product Form, Blocking, Transportation and Loss queues).

Module I: (L- 07)
Transportation and Loss Queues: State dependent M/G/c/c queues and queuing network models incorporating micro and macro aspects of traffic flow to capture throughput volume, speeds, density and congestion in transportation systems.

Module III: (L- 07)
Open Queuing Network Algorithms: Topological network design and computer implementation for performance and optimization of Product Form (Jackson) network, Non-Product Form networks (queuing network approximation algorithm of Whitt), Blocking networks (Expansion method for exponential blocking, generalized expansion method for more general distributions).

Module IV: (L- 08)
Closed Queuing Network Performance Models: Product Form networks (Gordon and Newell algorithms), Non-Product Form networks through generalized service time distributions, closed queuing analysis of Blocking networks, movement of goods from one queue to another in closed transportation and loss networks.

Module V: (L- 08)
Optimal Resource Allocation Problems in Topological Network Design: Resource allocation problems in improving stochastic flow process, Accessibility and egress addressed</td></tr>
</table>

	optimal routing optimization in design of queues, Optimal topology problems examined through integer and non-linear programming aspects (fixed and spatially generated topology).
Text Books, and/or reference material	Text Book: [T1]. Introduction to Queuing Networks, Theory and Practice – Smith, J. MacGregor (Springer). Reference Book: [R1]. Data Networks – D. Bertsekas and R. Gallager (Prentice Hall).

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<tr><th rowspan="2">Course Code</th><th rowspan="2">Title of the course</th><th rowspan="2">Program Core (PCR) / Electives (PEL)</th><th colspan="4">Total Number of contact hours: 41</th><th rowspan="2">Credit</th></tr>
<tr><th>Lecture (L)</th><th>Tutorial (T)</th><th>Practical (P)</th><th>Total Hours</th></tr>
<tr><td>EC9018</td><td>Image Processing</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Prerequisites</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="3">Signals and Systems, Digital Electronics, Digital Signal Processing</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Understand image enhancement and restoration techniques.
CO#2: Analyze digital images through multiresolution techniques.
CO#3: Understand the application of morphological processing and segmentation in digital images.
CO#4: Interpret digital image recognition techniques.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture Hours: 41

Module I: (L-04)
Digital Image Fundamentals: Image acquisition, Sampling, Quantization, Resolution, Relationship between pixels, Geometric transforms, Convolution and Correlation.

Module II: (L-07)
Image Enhancement: Gray level intensity transforms, Histogram processing, Image sharpening and smoothening operations (spatial and frequency based).

Module III: (L-05)
Image Restoration: Model of image degradation, Noise models, Restoration in the presence of noise only spatial filtering, Periodic noise reduction by frequency domain filtering, Estimating the degradation function, Weiner filtering, Constrained least squares filtering, Image interpolation and resampling.

Module IV: (L-05)
Multi-resolution Image Processing: Short time Fourier transform, Wavelet function, Wavelet series, Discrete wavelet transform and multi-resolution analysis, Image decomposition and compression using discrete wavelet transform.

Module V: (L-04)
Compression and Encoding of Image: Redundancy, Entropy coding, Lossy compression, Lossless compression, Quality preserving adaptive compression.

Module VI: (L-04)
Morphological Processing: Dilation and erosion, Opening and closing, Hit or Miss transform, Algorithms for feature extraction.

Module VII: (L-06)
Image Segmentation: Detection of discontinuities, Edge linking and boundary detection, Thresholding, Region based segmentation, Segmentation by morphological watersheds, Use of motion in segmentation.

Module VIII: (L-06)
Patterns in Images and their Applications: Basics of features, Principal component analysis, Decision tree and feature hierarchy, Scale invariant feature transform, Histogram of oriented gradient.</td></tr>
</table>

Text Books, and / or reference material	Text Books: 1. Digital Image Processing: R C Gonzalez and R E Woods; Pearson Education. 2. Guide to Signals and Patterns in Image Processing- Foundations, Methods and Applications: Apurba Das; Springer. 3. Digital Image Processing and Computer Vision: Sonka, Hlavac and Boyle; Cengage Learning (India Edition). Reference Books: 1. Digital Image Processing: K R Castleman; Pearson Education. 2. Digital Image Processing: S Sridhar; Oxford Higher Education.

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<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC 9024</td><td>Satellite Communication</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="3">Knowledge in Electromagnetic fields with problem solving capability (studied in EM Theory), Analog and Digital Communication, Introductory knowledge on information theory and coding</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: To compute the satellite orbit parameters, design orbits and can be able to classify them based on Kepler’s six elements.
CO2: Understand the concept of satellite launching and positioning of satellites in orbits
CO3: Can do computations of link design and classify different losses in propagation for space communication.
CO4: Assimilate the concept of multiple accessing techniques in satellite communication.
CO5: Develop ability to classify different types of application of satellite communication.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module I: (L- 02)
Historical background, Basic concepts, Frequency allocation for satellite services, orbital & spacecraft problems, comparison of networks and services, modulation techniques used for satellite communication. Spectrum Management (2L)

Module II: (L- 08)
Orbits- Two body problem, orbital mechanics, geostationary orbit, change in longitude, orbital manoeuvres, orbital transfer, and orbital perturbations. Launch Vehicles- principles of Rocket propulsion, powered flight, Launch vehicles for communication satellite

Module III: (L- 08)
RF link- noise, the basic RF link, satellite links (up and down) , optimization RF link, inter satellite link, noise temperature, Antenna temperature, overall system temperature, propagation factors, rain attenuation model. Tropospheric and Ionospheric effect. (8L)

Module VI: (L- 08)
Satellite subsystems and satellite link design- Altitude and orbit control (AOC) Subsystem, TT&C, power system, spacecraft antenna, transponder, Friis transmission equation, G/T ratio of earth station.

Module V: (L- 08)
Multiple access- FDMA, TDMA, CDMA techniques, comparison of multiple access techniques, error connecting codes.

Module VI: (L- 06)
Application of satellite in remote sensing and surveillance; Basic of remote sensing, Electromagnetic Radiation principles, Atmospheric window, Indian satellite sensing satellite system, Active, Passive, ground based and space based remote sensing.</td></tr>
</table>

Text Books, and/or reference material	**Text Books** [1] Dennis Roddy, *Satellite Communication*, 4/e, McGraw Hill [2] Louis J. Ippolito, Jr.*SatelliteCommunications Systems Engineering: Atmospheric Effects, Satellite Link Design and System Performance,* Second Edition. **Reference Books** [3] Recommendation ITU-R P.618-11, P Series Radio Wave Propagation. [4] Pratt and Bostian, *Satellite Communication*, 2/e, John Wiley and Sons. [5] Floyd F. Sabins, *Remote Sensing: Principles and Interpretation*, 3rd edition (August 1996), W H Freeman & Co. [6] Tri T Ha, *Digital Satellite Communication*, McGraw Hill

EC9024: Satellite Communication (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	Program Outcomes					
		PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	To compute the satellite orbit parameters, design orbits and can be able to classify them based on Kepler's six elements.	**1**	**1**	**2**	**2**	**3**	**1**
CO2	Understand the concept of satellite launching and positioning of satellites in orbits	**3**	**2**	**3**	**2**	**1**	**2**
CO3	Can do computations of link design and classify different losses in propagation for space communication.	**2**	**1**	**3**	**1**	**2**	**1**
CO4	Assimilate the concept of multiple accessing techniques in satellite communication.	**2**	**2**	**3**	**2**	**2**	**2**
CO5	Develop ability to classify different types of application of satellite communication.	**1**	**3**	**2**	**2**	**1**	**3**

<table>
<tr><td></td><td></td><td></td><td colspan="4"></td><td></td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC 9025</td><td>Microwave Circuits and Techniques</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="3">Knowledge in Electromagnetic fields with problem solving capability (studied in EM Theory), Analog circuits, Optional acquaintance to a preliminary course of microwave engineering.</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Students will be able to learn the intricacies of design constraints at high frequency.
CO#2: The basic training for understanding circuit design at microwave frequencies for our Country’s defense and space applications would be enriched.
CO#3: The students can design planar circuits and can provide reasoning for the obtained results.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module I: (02)
Introduction: Microwave and mm wave spectrum, Typical applications of microwave and mm wave, Safety considerations. Difference in High frequency and relatively low frequency behaviour of Lumped circuit components. Miniaturization and design of Lumped components at high RF. Realization of reactive elements as microwave and mm wave planar circuit components.[1][2]

Module II: (L- 04)
Review of Transmission line theory. Concept of Scattering Matrix N-port networks-Properties of S matrix, Transmission matrix and their relationships

Module III: (L- 06)
Microwave and mm wave Waveguide and Resonators: Rectangular Waveguide- design consideration, TE and TM modes, TE_{10} mode analysis, cut-off frequency, propagation constant, intrinsic wave impedance, phase and group velocity, power transmission, attenuation, waveguide excitation, wall current; Introduction of circular waveguide; Rectangular waveguide resonator design consideration, resonant frequency, Q-factor, excitation.[1][3]

Module IV: (L- 06)
Planar Transmission lines and Resonators: Propagation characteristics, comparison for different characteristics of the above mentioned lines. strip line, micro-strip line, coplanar waveguide, Slot line-design consideration, Substrate integrated waveguide, non radiating dielectric guides, Design synthesis and analysis[1][2]

Module V: (L- 08)
Passive Components and their S-matrix Representation: Microwave and mm wave passive components and their S matrix representation: Attenuators, Phase shifter, Directional coupler, Bethe-hole coupler, magic tee, hybrid ring, circulators, Isolators; design of planar power dividers and couplers; design procedure of filter using insertion loss method-specification, low-pass prototype design, scaling and conversion, implementation. [2][3]

Module VI: (L- 06)</td></tr>
</table>

	Microwave and mm wave devices and Application to switches and mixers: TED (Gunn diode) & Avalanche Transit Time (IMPATT) device, Schottky diode, PIN & applications; Microwave bipolar transistor, Microwave field effect transistor. [2] **Module VII: (L- 06)** **Microwave Amplifier Design:** Basic consideration in the design of microwave amplifier-transistor S-parameter, Stability, matching network, noise figure; matching network design using lumped elements and L-Section. Design of LNA.[1][4] **Module VIII: (L- 04)** **Microwave and mm wave measurement basics:** VSWR meter, tunable detector, slotted line and probe detector, spectrum analyzer, network analyzer, measurement of VSWR – low, medium and high, measurement of power: low, medium and high, frequency measurement.[1][4]
Text Books, and/or reference material	**Text Books:** [1] David. M. Pozar, *Microwave Engineering*, 2/e, 1998 (John Wiley & Sons). [2] R Ludwig and P Bretchko, *RF Circuit Design: Theory and Application*, Pearson Education, New Delhi [3] Samuel Y Liao, *Microwave Devices and Circuits*, 3/e, PHI. [4] Sisodia and Raghuvanshi, *Microwave Circuits and Passive Devices*, New Age International [5] G H Bryant, *Principles of microwave Measurement*, London : P. Peregrinus Ltd. on behalf of the Institution of Electrical Engineers, c1988 **Reference Books:** [1] P A Rizzi, *Microwave Engineering: Passive Circuits*, 2000, PHI [2] R E Collin, *Foundations of Microwave Engineering*, John Wiley and Sons India Pvt. Ltd.

EC 9025: Microwave Circuits & Techniques (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Students will be able to learn the intricacies of design constraints at high frequency.	2	1	2	2	3	1
CO 2	The basic training for understanding circuit design at microwave frequencies for our Country's defense and space applications would be enriched.	2	3	1	1	3	1
CO 3	The students can design planar circuits and can provide reasoning for the obtained results.	3	2	1	1	3	1
Average		**2.3**	**2.0**	**1.3**	**1.3**	**3.0**	**1.0**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)/OEL</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9036</td><td>EMBEDDED SYSTEMS</td><td>PEL</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="3">Basic Electronics, Mechanics</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO#1: Understand concept of contemporary Embedded systems
CO#2: Apply analysis techniques to physical systems
CO#3: Understand case study in Embedded system
CO#4: Design of Embedded systems</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module I: (L- 02)
Introduction to Embedded systems: Motivation based on applications of embedded systems, Basics of Embedded systems, functional blocks

Module II: (L- 08)
Modeling of Embedded system: Mathematical modeling of physical systems to fit into embedded systems, Continuous Dynamics, Discrete Dynamics, Hybrid Systems, actor models, Composition of State Machines

Module III: (L- 04)
Cyber physical system architecture and Industry 4.0, Background of Industry standards, Cyber physical system, IoT, Industry 3.0, Industry 4.0

Module IV: (L- 14)
Microcontrollers, Sensors, Actuators, Basics of Microcontrollers, 8951, Arduino microcontroller development board, I/Os, Sensors, Actuators

Module V: (L- 06)
Data networking, Data communication techniques, Internet, Ethernet, WiFi, Bluetooth and Cellular, LoRa

Module VI: (L- 06)
Case study in embedded system, Case study based on applications</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7"><u>Text Books</u>:
1. Introduction to Embedded Systems - a Cyber Physical Systems Approach, By Edward Ashford Lee, Sanjit Arun kumar Seshia
2. Principles of measurement systems. By Bentley
3. Industry 4.0 the industrial internet of things, by Alasdair Gilchrist
4. Data Communications And Networking (SIE) by Behrouz Forouzan
5. Class notes and Research Articles</td></tr>
</table>

EC 9036: Embedded Systems (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Understand concept of contemporary Embedded systems.	1	2	1	1	1	3
CO 2	Apply analysis techniques to physical systems.	2	1	2	2	1	3
CO 3	Understand case study in Embedded system.	2	1	2	1	2	3
CO 4	Design of Embedded systems.	1	2	1	1	1	3
Average		**1.5**	**1.5**	**1.5**	**1.3**	**1.3**	**3.0**

<table>
<tr><td colspan="8">Department of Electronics and Communication Engineering</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Title of the course</td><td rowspan="2">Program Core (PCR) / Electives (PEL)</td><td colspan="4">Total Number of contact hours: 40</td><td rowspan="2">Credit</td></tr>
<tr><td>Lecture (L)</td><td>Tutorial (T)</td><td>Practical (P)</td><td>Total Hours</td></tr>
<tr><td>EC9038</td><td>Error Control Coding</td><td>PCR</td><td>4</td><td>0</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td colspan="3">Pre-requisites:</td><td colspan="5">Course Assessment methods (Class test/assignment, Mid-semester and End assessment (EA))</td></tr>
<tr><td colspan="3">Linear Algebra, Probability, Communication Engineering</td><td colspan="5">CT+MA+EA</td></tr>
<tr><td>Course Outcomes</td><td colspan="7">CO1: Acquire idea about different types of error control coding techniques.
CO2: Understand generator matrix, encoding and decoding of different codes.
CO3: Learn LDPC, BCH, RS and Turbo codes.
CO4: Analyze and mitigate errors in channels.
CO5: Differentiate between different coding strategies.</td></tr>
<tr><td>Topics Covered</td><td colspan="7">Total Lecture hours: 40

Module I: (L- 09)
Introduction to Linear Algebra: Group, Ring, Field, Vector Space.

Module II: (L- 10)
Binary Linear Block Codes: Generator and Parity Check Matrices, Dual Codes, Decoding, General properties of linear block codes, Hamming Code.

Module III: (L- 04)
Cyclic Codes: Algebraic description, Encoding and Decoding of Cyclic codes.

Module IV: (L- 03)
BCH Codes: Properties, Encoding and Decoding.

Module V: (L- 01)
Reed Solomon (RS) Codes: Definition, Decoding of RS codes.

Module VI: (L- 07)
Convolution Codes: Definition, Encoding Trellis and State representation, Viterbi decoding, Error probability.

Module VII: (L- 03)
LDPC Codes : Definition, Construction, Regular and irregular LDPC, Belief Propagation, Tanner Graph, Decoding, Iterative Decoding

Module VIII: (L- 03)
Turbo Codes: Definition, Construction methods, Decoding</td></tr>
<tr><td>Text Books, and/or reference material</td><td colspan="7">Text Books:
1. Error Control Coding; Fundamentals and applications: Shu Lin and Daniel. J. Costello Jr. Second Edition, Pearson India.

2. Essentials of Error Control Coding by Moreira and Farrel, Wiley India
Reference Books:</td></tr>
</table>

	1. Error Correction Coding: Mathematical Methods and Algorithms by Todd.K. Moon, Wiley India.

EC 9038: Error Control Coding (Elective)
[Mapping between course outcomes (COs) and program outcomes (POs)]

CO	Statement	PO 1	PO 2	PO 3	PSO 1	PSO 2	PSO 3
CO 1	Acquire idea about different types of error control coding techniques.	3	1	1	3	2	1
CO 2	Understand generator matrix, encoding and decoding of different codes.	2	2	2	3	1	2
CO 3	Learn LDPC, BCH, RS and Turbo codes.	2	2	1	3	1	2
CO 4	Analyze and mitigate errors in channels.	3	1	3	3	1	1
CO 5	Differentiate between different coding strategies.	1	1	2	3	2	2
Average		**2.2**	**1.4**	**1.8**	**3.0**	**1.4**	**1.6**